The Section 103 Rejections

Turning now to the rejections under 35 USC 103 (a), Applicant requests reconsideration as the rejections of Claims 1-15 are unfounded.

The invention of Claim 1 concerns a DMOS device. While the claim speaks for itself, a reading shows that Claim 1 is directed towards "a method for forming a body region in a drain region of a DMOS device on a wafer after a gate of the DMOS device has been formed." The method provides for the forming of the body region in the drain region so that the body region extends "partly beneath the gate of the DMOS device" and is "appropriately aligned with the gate." The method of Claim 1 is a two-step method which requires:

> "(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and
> (b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region. . ."

The steps (a) and (b) may be performed in any order. The method additionally requires that:

- the dopant is implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, and
- the first angle to the surface plane at which the dopant is directed in step (a) is less than a second angle to the surface plane at which the dopant is directed in step (b).

Manifestly, none of the references, singly or in any acceptable combination, teaches or suggests a method for forming a body region in a drain region of a DMOS device on a wafer after a gate has been formed, with the body region extending partly beneath the gate of the DMOS device and appropriately aligned with the gate, according to the steps and limitations above noted with reference to Claim 1.

More specifically, claims 1-13 have been rejected as obvious over Han et al (U.S. Patent No. 5,409,848) in view of Hshieh (U.S. Patent No. 4,931,408). Notwithstanding the Examiner's initial statement of the rejection, the supporting discussion of the rejection makes clear that Hsieh (not Han) is actually the primary reference as the Examiner applies Han to modify or supplement Hshieh and not the other way around. Therefore we will first address Hshieh and then Han.

Hshieh discloses a method for forming a DMOS device, and for forming a P-body region in the device. However, Hshieh fails to disclose or suggest a method which includes the steps (a) and (b) of Claim 1. In Hshieh, the P-type impurities for forming the P-body region 64 are directed to the epitaxial layer 42 at one angle only, which is at 90° to the epitaxial layer. Hshieh relies on a subsequent diffusion step for diffusing the P-type impurities into the epitaxial layer 42 for forming the P-body region extending beneath the gate of the device. Furthermore, there is no suggestion in Hshieh of the possibility of forming the P-body region by a two-angle implantation process. The Examiner therefore seeks to combine with the teaching of Hshieh that of Han et al., in an effort to plug the hole i Hshieh's teaching.

Han (U.S. Patent No. 5,409,848) discloses a method for forming a P-type MOSFET. However, Han does not teach or suggest any method for forming a DMOS device. Further, it does not disclose or suggest any method for forming a body region in a drain region of a DMOS device on a wafer. Consequently, and contrary to the Examiner's reasoning, the disclosure of Han is not combinable with that of Hshieh. One

of ordinary skill in the art would not try to combine them; they relate to manifestly different kinds of devices.

Further, in Han's method, after the gate, the source and the drain have been formed, an N-type dopant is implanted to form regions 16 which extend beneath the source and drain and the gate oxide 13. The N-type dopant for forming the regions 16 may be arsenic and phosphorous and it is suggested that the dopant be implanted at an angle greater than zero from a line perpendicular from the surface of the substrate. A preferred angle from the vertical is 45°, although angles in the range of 5° to 75° from the vertical are suggested as being suitable. However, Applicant again emphasizes that Han does not disclose or suggest any method for forming a body region in a drain region of a DMOS device. It also does not disclose or suggest the formation of any region in a device where the dopant or dopants for forming the region are implanted at different angles. In the formation of the regions 16, the dopant, while it is directed at an angle to the vertical, is directed at one angle and one angle only - in stark contrast to all of Applicant's claims.

Accordingly, in his method for forming a P-type MOSFET, Han fails to disclose or suggest the possibility of forming any region in the MOSFET by implantation where the dopant or dopants are directed in two steps at different angles one to the other.

In other words, even were the teachings of Han and Hshieh combined (which would not be proper, as explained below), the result would not be the invention of any of claims 1-13.

Moreover, the proposed motivation for effecting the combination is improper and reflects no more than impermissible hindsight. The Examiner is required to provide a factual foundation for a conclusion that those skilled in the art would have found somewhere - in one of the references or in their knowledge base - not just knowledge

that the references could be combined, but, rather, a motivation to do so. The Examiner appears to be using the present inventor's own motivations and attributing them to others, which is clearly improper. This argument does not satisfy the Examiner's burden as recently reiterated by the Court of Appeals for the Federal Circuit in In re Lee. A conclusion of motivation to combine references must rest on a proper factual foundation.

The rejection of claims 1-13 thus must be withdrawn.

Next, the Examiner rejects claims 14 and 15 as obvious over the combination of Hshieh, Han and Contiero et al. As claims 1-13 are allowable in light of the points made above, and claims 14-15 are dependent, they likewise are allowable without more being said. Nevertheless, for completeness, we address the rejection as though claims 1-13 still stand rejected.

Even if Han were combinable with Hshieh and Contiero, which it is not, as explained above, Han does not disclose or suggest the possibility of implanting a dopant in two implantation steps at different angles, one to the other, for forming a region in his MOSFET.

The Examiner has also referred to the discussion of the prior art in the specification of Han. None of the prior art documents discussed by Han in his specification, with the exception to the reference to U.S. Patent Specification No. 4,931,408 of Hshieh at Column 5, relate to the fabrication of DMOS devices. Furthermore, none teaches or suggests any method for forming a body region in a drain region of a DMOS device wafer after a gate has been formed. Additionally, none of the documents discussed in Han disclose or suggest a method for forming a body region in a drain region of a DMOS device on a wafer after a gate has been formed with the body region partly beneath the gate of the DMOS device and appropriately aligned with the

gate which comprises implanting a dopant in two steps in order to provide a desired drain/source threshold voltage and a desired breakdown voltage in which the implanting angles are different for the respective steps.

Therefore, even if Han were combinable with Hshieh and Contiero, which it is not, as the motivation is lacking, one would not have sufficient teaching to arrive at the invention of Claim 1.

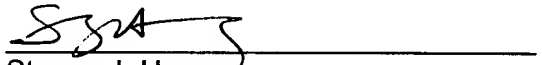
Contiero, in the article titled "LDMOS IMPLEMENTATION BY LARGE TILT IMPLANT IN 0.6 μm BCD5 PROCESS, FLASH MEMORY COMPATIBLE" read at the international symposium of Power Semi-conductor Devices in May 1996 and discussed in the instant specification at Page 2, Line 1 to Page 3, Line 10, also fails to disclose or suggest the invention of Claim 1. Contiero discloses a method for fabricating an LDMOS device in which the P-body region is formed beneath the gate by implanting an appropriate dopant into the drain region at an angle to the surface of the drain region. The edge of the gate is used to form a mask on the drain region. However, as discussed in the present specification, Contiero only discloses implantation of the dopant for forming the P-body region at a single angle. Contiero et al suggest that the implantation to form the P-body region may be carried out at a tilt angle of any one of 30°, 40°, 45° and 60°, and suggest that a 45° tilt angle is preferable. However, in the method of Contiero the dopant is implanted at one single angle and one angle only to form the P-body region. There is no disclosure, nor is there any suggestion, in the paper of Contiero of the possibility of carrying out the implantation for forming the P-body region as a two-step process using two different angles of implantation.

The only justification for the combination of the references is hindsight, which may not be used. Even then, the combined teachings of the references do not bring one to the claimed invention. The result of the combination would not be, inter alia, a two-step process using two different angles of implantation. Consequently, the

invention of Claims 14 and 15 (as well as that of claims 1-13) is not obvious, and should be allowed, over the references of record.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,



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Marked-up claims

1. (Amended) A method for forming a body region in a drain region of a DMOS device on a wafer after [the] a gate has been formed with the body region extending partly beneath [a] the gate of the DMOS device and appropriately aligned with the gate, the drain region defining a surface plane, the method comprising the steps of:

(a) implanting a suitable dopant in a portion of the drain region adjacent the gate for forming the body region to have a desired drain/source threshold voltage, and

(b) implanting a suitable dopant in the said portion of the drain region adjacent the gate for forming the body region to have a desired breakdown voltage through the drain region,

steps (a) and (b) being performed in any order, and the dopant being implanted in step (a) by directing the dopant at a first angle to the surface plane of the drain region for directing at least some of the dopant beneath the gate, the first angle to the surface plane at which the dopant is directed in step (a) being less than a second angle to the surface plane at which the dopant is directed in step (b).

13. (Amended) A method as claimed in Claim 1 in which the dose and energy levels of the dopant implanted in each of steps (a) and (b) are sufficient for providing the desired drain/source threshold voltage and the desired breakdown voltage through the drain region.